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09/725,704	11/29/2000	Thomas J. Cloonan	4807.00017	8828

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ARRIS INTERNATIONAL, INC
3871 LAKEFIELD DRIVE
SUWANEE, GA 30024

EXAMINER	
PARRY, CHRISTOPHER L	
ART UNIT	PAPER NUMBER
2623	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/725,704	CLOONAN ET AL.	
	Examiner	Art Unit	
	CHRIS PARRY	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date. _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 17 December 2007 have been fully considered but they are not persuasive.

In response to applicant's argument (Page 9, 2nd ¶, lines 1-2) stating, Lovett does not teach copying a future timing value from one device to another to synchronize the clock of the other with the first device, the examiner respectfully disagrees. Lovett discloses secondary node (i.e. node 12) is synchronized with a source node, such as node 13. Lovett further teaches loading the timing value from base register 108 to write register 82 and adding an offset value (i.e., future value) at adder 84 and stores the future value to clock register 86 (Col. 5, line 59 to Col. 6, line 39). Lovett discloses adding this offset at the secondary node rather than copying the offset from the source node to the secondary node. However Lovett in combination with Eatherton discloses adding a delay time or offset value to the counter value and copying the future value from the master component to the all components (Eatherton – Col. 3, line 40 to Col. 4, line 60).

In response to applicant's argument (Page 9, 3rd ¶, line 1) stating, Lovett does not disclose copying a future timing value, the examiner respectfully disagrees. As stated above, an offset value is added to the current timing value and is stored in clock register 86 (Col. 5, line 59, to Col. 6, line 39).

In response to applicant's argument (Page 9, 4th ¶, lines 4-5) stating, Lovett teaches away from "copying said future timing counter value into the storage devices that is local with respect to the second cable interface circuit", the examiner respectfully disagrees. Lovett teaches adding an offset delay to timing value received from base register 108 of the source node at adder 84 of the second node, then loading the new timing value or "future value" to clock register 86 (i.e., local storage device) of the local node (Col. 5, line 59 to Col. 6, line 39).

In response to applicant's argument (Page 9, 5th ¶, lines 1-2) stating, combining Lovett with sale does not result in a likelihood of success in arriving at the claimed subject matter, the examiner respectfully disagrees. Salee teaches a system for increased headend reliability in a cable network system through synchronized redundancy in media access components, while Lovett teaches providing a system with distributed local clocks wherein a local clock may be synchronized with other clocks in the system. Thus, Salee is analogous to Lovett has both discuss methods of synchronizing clocks within computer chips.

In response to applicant's argument (Page 11, 2nd ¶, lines 1-7) that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Eatherton could not provide the level of synchronization with 500 nsec of accuracy) are not recited in the rejected claim(s).

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument (Page 12, 2nd ¶, lines 1-8) stating that Eatherton does not disclose trigger signals, the examiner respectfully disagrees. Eatherton teaches the master component (system controller) initializes an update timer which is used to determine when to update the packet switching system (interface cards) with the global time (Col. 6, lines 22-27). Therefore, when the master component determines to update the packet switching system with a new global time, master component sends out a trigger signal to all components to update local clocks. The global time includes an offset delay for the time required to transmit the trigger signal (Col. 3, line 61 to Col. 5, line 61).

In response to applicant's argument (Page 12, 4th ¶, lines 1-5) that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Eatherton teaches an improved method for synchronizing a representation of time

between components of a packet switching system which is analogous to the systems of Salee and Lovett.

Claim Objections

2. Claims 12-14 are objected to because of the following informalities: In line 1 of claims 12-14, "cable modern" should be changed to --cable modem--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 12-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 12-14 recite the limitation "the master" in line 11 of each claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salee (US Pub. No. 2002/0088003 A1) [cited in previous action] in view of Lovett et al. "Lovett" (USPN 6,591,370) [cited in previous action] in view of Eatherton (USPN 6,697,382) [cited in previous action].

Regarding Claim 12, Salee discloses a cable modem termination system (CMTS) with a plurality of cable interface circuits (10, 20 – figure 1, ¶ 12) each of which includes a cyclical timing counter (24 – figure 1) that provides timing signals to cable modems (CMs) coupled to each of said interface circuits (¶¶ 12-13), a method of synchronizing the timing counters (24) of a first cable interface circuit (10) and a second cable interface circuit (20) comprised of the steps of:

copying a first value (P) of said timing counter (24) of said first cable interface circuit (10) into a storage device (26) (¶ 14);

copying said first timing counter value (P) into the storage device (26) that is local with respect to the second cable interface circuit (20) (¶ 14); and

copying the value from said storage device (26) that is local with respect to the second cable interface circuit (20) into said timing counter (24) of said second cable interface circuit (20) (¶ 14).

Salee fails to disclose adding an offset to the first timing value, such that the value copied into the storage device local to the second cable interface card is a future timing counter value, i.e., the sum of the first timing counter value and the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit.

In an analogous art, Lovett discloses a method of synchronizing the timing counters of a first circuit (13) and a second circuit (12) (Col. 3, line 65 - Col. 4, line 7) comprising the steps of:

copying a first timing counter value of the first circuit (source node) into a storage device (108) (Col. 6, lines 1-7);

adding an offset (elapsed time) to said first timing counter value to create a future timing counter value, the future timing counter value being the sum of said first timing counter value and the offset (Col. 6, lines 22-27), wherein the offset amount includes the time to transfer the first timing counter value from the master timing counter into the storage device local to the second circuit (Col. 6, lines 20-22);

copying said first timing counter value into the storage device (82) that is local with respect to the second circuit (node being synchronized) (Col. 6, lines 16-18); and

copying said future timing counter value into the timing counter (86) of said second circuit (Col. 6, lines 27-30).

Lovett further discloses that the disclosed method enables circuits to be added to the system without effecting the synchronization of the other circuits in the system (Col. 6, lines 33-39), thereby preventing disruption of current packet-based communications sessions executing on system nodes (Col. 1, lines 48-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee to include adding an offset to the first timing value copied into the storage device local to the second cable interface card to create a future timing counter value that is the sum of the first timing counter value and

the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit, for the benefit of enabling new cable interface circuits to be added and synchronized to the first cable interface circuit without disrupting current communication sessions executing on active cable interface circuits.

Salee in view of Lovett fails to disclose that the offset is added to the first timing counter value before said first timing counter value is copied to the storage device local to the second cable interface circuit and the step of copying said future timing counter value from said first cable interface circuit to second cable interface circuit.

In an analogous art, Eatherton discloses a method of synchronizing timing counters of first and second interface circuits (169, 179) in a packet switching system (Col. 3, lines 40-57).

Similar to Lovett, Eatherton discloses adding an offset (delay) to a first timing counter value (global time) to create a future timing counter value, wherein the offset amount includes the time to transfer a timing value from the first timing counter (313) of the first interface circuit (310) into a storage device (324) local to the second interface circuit (320) (Col. 3, lines 61-66; Col. 4, line 38 - Col. 5, line 61).

Eatherton further discloses that the future timing counter value is created prior to copying said future timing value into the storage device that is local to the second interface circuit (Col. 3, line 66 to Col. 4, line 1; Col. 4, lines 21-23), thus reducing the number of steps carried out at the second interface circuit during the synchronization process.

Eatherton teaches wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of:

waiting a predetermined length of time (i.e., the predetermined update delay, Eatherton, Col. 4, lines 56-58) until said timing counter of the first cable interface circuit is substantially equal to said future timing counter value (Col. 6, line 60 - Col. 7, line 7); and

copying said future timing counter value from said storage device into said timing counter of the second cable interface circuit (Col. 6, line 60 - Col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee in view of Lovett to include adding the offset to the first timing counter value to create a future timing counter value and copying said future timing counter value into the storage device local to the second cable interface circuit, as taught by Eatherton, for the benefit of simplifying the synchronization process as carried out by the second cable interface circuit.

Regarding Claim 13, Salee discloses a cable modem termination system (CMTS) with a plurality of cable interface circuits (10, 20 – figure 1, ¶ 12) each of which includes a cyclical timing counter (24 – figure 1) that provides timing signals to cable modems (CMs) coupled to each of said interface circuits (¶¶ 12-13), a method of synchronizing the timing counters (24) of a first cable interface circuit (10) and a second cable interface circuit (20) comprised of the steps of:

copying a first value (P) of said timing counter (24) of said first cable interface circuit (10) into a storage device (26) (¶ 14);

copying said first timing counter value (P) into the storage device (26) that is local with respect to the second cable interface circuit (20) (¶ 14); and

copying the value from said storage device (26) that is local with respect to the second cable interface circuit (20) into said timing counter (24) of said second cable interface circuit (20) (¶ 14).

Salee fails to disclose adding an offset to the first timing value, such that the value copied into the storage device local to the second cable interface card is a future timing counter value, i.e., the sum of the first timing counter value and the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit.

In an analogous art, Lovett discloses a method of synchronizing the timing counters of a first circuit (13) and a second circuit (12) (Col. 3, line 65 - Col. 4, line 7) comprising the steps of:

copying a first timing counter value of the first circuit (source node) into a storage device (108) (Col. 6, lines 1-7);

adding an offset (elapsed time) to said first timing counter value to create a future timing counter value, the future timing counter value being the sum of said first timing counter value and the offset (Col. 6, lines 22-27), wherein the offset amount includes the time to transfer the first timing counter value from the master timing counter into the storage device local to the second circuit (Col. 6, lines 20-22);

copying said first timing counter value into the storage device (82) that is local with respect to the second circuit (node being synchronized) (Col. 6, lines 16-18); and

copying said future timing counter value into the timing counter (86) of said second circuit (Col. 6, lines 27-30).

Lovett further discloses that the disclosed method enables circuits to be added to the system without effecting the synchronization of the other circuits in the system (Col. 6, lines 33-39), thereby preventing disruption of current packet-based communications sessions executing on system nodes (Col. 1, lines 48-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee to include adding an offset to the first timing value copied into the storage device local to the second cable interface card to create a future timing counter value that is the sum of the first timing counter value and the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit, for the benefit of enabling new cable interface circuits to be added and synchronized to the first cable interface circuit without disrupting current communication sessions executing on active cable interface circuits.

Salee in view of Lovett fails to disclose that the offset is added to the first timing counter value before said first timing counter value is copied to the storage device local to the second cable interface circuit and the step of copying said future timing counter value from said first cable interface circuit to second cable interface circuit.

In an analogous art, Eatherton discloses a method of synchronizing timing counters of first and second interface circuits (169, 179) in a packet switching system (Col. 3, lines 40-57).

Similar to Lovett, Eatherton discloses adding an offset (delay) to a first timing counter value (global time) to create a future timing counter value, wherein the offset amount includes the time to transfer a timing value from the first timing counter (313) of the first interface circuit (310) into a storage device (324) local to the second interface circuit (320) (Col. 3, lines 61-66; Col. 4, line 38 - Col. 5, line 61).

Eatherton further discloses that the future timing counter value is created prior to copying said future timing value into the storage device that is local to the second interface circuit (Col. 3, line 66 to Col. 4, line 1; Col. 4, lines 21-23), thus reducing the number of steps carried out at the second interface circuit during the synchronization process.

Eatherton teaches wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of:

waiting a predetermined length of time (i.e., the predetermined update delay, Eatherton, col. 4, 11. 56-58) until said timing counter of the first cable interface circuit increases to a value substantially equal to said future timing counter value (Col. 6, line 60 - Col. 7, line 7); and

copying said future timing counter value from said storage device into said timing counter of the second cable interface circuit (Col. 6, line 60 - Col. 7, line 7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee in view of Lovett to include adding the offset to the first timing counter value to create a future timing counter value and copying said future timing counter value into the storage device local to the second cable interface circuit, as taught by Eatherton, for the benefit of simplifying the synchronization process as carried out by the second cable interface circuit.

Regarding Claim 14, Salee discloses a cable modem termination system (CMTS) with a plurality of cable interface circuits (10, 20 – figure 1, ¶ 12) each of which includes a cyclical timing counter (24 – figure 1) that provides timing signals to cable modems (CMs) coupled to each of said interface circuits (¶¶ 12-13), a method of synchronizing the timing counters (24) of a first cable interface circuit (10) and a second cable interface circuit (20) comprised of the steps of:

copying a first value (P) of said timing counter (24) of said first cable interface circuit (10) into a storage device (26) (¶ 14);

copying said first timing counter value (P) into the storage device (26) that is local with respect to the second cable interface circuit (20) (¶ 14); and

copying the value from said storage device (26) that is local with respect to the second cable interface circuit (20) into said timing counter (24) of said second cable interface circuit (20) (¶ 14).

Salee fails to disclose adding an offset to the first timing value, such that the value copied into the storage device local to the second cable interface card is a future

timing counter value, i.e., the sum of the first timing counter value and the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit.

In an analogous art, Lovett discloses a method of synchronizing the timing counters of a first circuit (13) and a second circuit (12) (Col. 3, line 65 - Col. 4, line 7) comprising the steps of:

copying a first timing counter value of the first circuit (source node) into a storage device (108) (Col. 6, lines 1-7);

adding an offset (elapsed time) to said first timing counter value to create a future timing counter value, the future timing counter value being the sum of said first timing counter value and the offset (Col. 6, lines 22-27), wherein the offset amount includes the time to transfer the first timing counter value from the master timing counter into the storage device local to the second circuit (Col. 6, lines 20-22);

copying said first timing counter value into the storage device (82) that is local with respect to the second circuit (node being synchronized) (Col. 6, lines 16-18); and

copying said future timing counter value into the timing counter (86) of said second circuit (Col. 6, lines 27-30).

Lovett further discloses that the disclosed method enables circuits to be added to the system without effecting the synchronization of the other circuits in the system (Col. 6, lines 33-39), thereby preventing disruption of current packet-based communications sessions executing on system nodes (Col. 1, lines 48-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee to include adding an offset to the first timing value copied into the storage device local to the second cable interface card to create a future timing counter value that is the sum of the first timing counter value and the offset, wherein the offset amount includes the time to transfer a timing value from the first timing counter into a storage device local to the second cable interface circuit, for the benefit of enabling new cable interface circuits to be added and synchronized to the first cable interface circuit without disrupting current communication sessions executing on active cable interface circuits.

Salee in view of Lovett fails to disclose that the offset is added to the first timing counter value before said first timing counter value is copied to the storage device local to the second cable interface circuit and the step of copying said future timing counter value from said first cable interface circuit to second cable interface circuit.

In an analogous art, Eatherton discloses a method of synchronizing timing counters of first and second interface circuits (169, 179) in a packet switching system (Col. 3, lines 40-57).

Similar to Lovett, Eatherton discloses adding an offset (delay) to a first timing counter value (global time) to create a future timing counter value, wherein the offset amount includes the time to transfer a timing value from the first timing counter (313) of the first interface circuit (310) into a storage device (324) local to the second interface circuit (320) (Col. 3, lines 61-66; Col. 4, line 38 - Col. 5, line 61).

Eatherton further discloses that the future timing counter value is created prior to copying said future timing value into the storage device that is local to the second interface circuit (Col. 3, line 66 to Col. 4, line 1; Col. 4, lines 21-23), thus reducing the number of steps carried out at the second interface circuit during the synchronization process.

Eatherton teaches wherein said step of copying said future timing counter value from said storage device into said timing counter includes the steps of: triggering the transfer of said future timing counter value from said storage device into said timing counter from a System Controller for said CMTS (Col. 6, lines 23-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Salee in view of Lovett to include adding the offset to the first timing counter value to create a future timing counter value and copying said future timing counter value into the storage device local to the second cable interface circuit, as taught by Eatherton, for the benefit of simplifying the synchronization process as carried out by the second cable interface circuit.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRIS PARRY whose telephone number is (571) 272-8328. The examiner can normally be reached on Monday through Friday, 8:00 AM EST to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Grant can be reached on (571) 272-7294. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CHRIS PARRY
Examiner
Art Unit 2623

/C. P./
Examiner, Art Unit 2623

/Christopher Grant/
Supervisory Patent Examiner, Art Unit 2623